Course Title: **Computer Architecture**
Course No. : ICT. Ed
Level: M.Ed.
Semester: First

Nature of course: Theoretical
Credit Hour: 3 hours
Teaching Hour: 75 hours(45+30)

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1. Course Description

This course is an introduction to computer architecture and organization. It covers topics in both the physical design of the computer (organization) and the logical design of the computer (architecture). This course discusses the basic structure of a digital computer and deals with the detail study of the organization of the Control unit, the Arithmetic and Logical unit, the Memory unit and the I/O unit.

2. General Objectives

The general objectives of this course are as follows:

- to provide the organization, architecture and designing concept of computer system including processor architecture, computer arithmetic, memory system, I/O organization and multiprocessors.
- to discuss in detail the operation of the arithmetic unit including the algorithms & implementation of fixed-point and floating-point addition, subtraction, multiplication & division.
- to study in detail the different types of control and the concept of pipelining.
- to study the hierarchical memory system including cache memories and virtual memory.
- To study the different ways of communicating with I/O devices and standard I/O interfaces.

3. Course Outlines

Specific Objectives	Contents	Teaching Hours
• Explain basic of SSI, MSI, LSI circuits, computer families, organization and future trends	**Unit I: Introduction** 1.1 SSI and MSI circuits 1.2 VLSI Technology 1.3 Mile stone in computer organization 1.4 Examples of computer families 1.5 Future trends in computer	**5**
• Explain Arithmetic and Logic unit, instruction sets, addressing modes and formats. • Understand processor and register organization, instruction cycle, Pentium processor and Power PC processor.	**Unit II: Central Processing unit: Case Study** 3.1 Arithmetic and Logic unit (ALU) 3.2 Instruction sets 3.3 Addressing modes and formats 3.4 Stack 3.5 Processor organization 3.6 Register organization 3.7 Instruction cycle 3.8 Pentium processor	**15**

	3.9 Power PC processor	
• Understand Micro-operations and control of CPU. • Explain hardwired implementation, micro-instruction sequencing and execution as well as application of micro-programming.	**Unit III: Control Unit Design** 3.1 Micro-operations 3.2 Control of CPU 3.3 Hardwired implementation, 3.4 Micro-instruction sequencing 3.5 Micro-instruction execution 3.6 Application of micro-programming	**15**
• Explain addition, subtraction, multiplication and division algorithms. • Elaborate different logical operations.	**Unit IV: Computer Arithmetic** 4.1 Addition algorithm 4.2 Subtraction algorithm 4.3 Multiplication algorithm 4.4 Division algorithm 4.5 Logical operation	**15**
• Explain the external devices and I/O modules • Elaborate programmed I/O, Interrupt driven I/O direct memory access, I/O channels and processors as well as the external interfaces.	**Unit V: Input/ Output Organization** 5.1 External devices 5.2 I/O modules 5.3 Programmed I/O 5.4 Interrupt Driven I/O Direct memory access 5.5 I/O channels and processors 5.6 External interfaces	**12**
• Explain the organization of main, auxiliary, associative, virtual and cache memory. • Elaborate on cache memory driving forces and cache design issues including placement, fetch, replacement and update policies	**Unit VI: Memory Organization** 6.1 Main memory, 6.2 Auxiliary memory, 6.3 Associative memory, 6.4 Virtual memory, 6.5 Cache memory, 6.6 Cache memory driving forces, 6.7 Cache design issues, 6.8 Placement, Fetch, Replacement & Update policies.	**12**
• Differentiate between RISC and CISC systems. • Explain RISC instructions, processor to memory movement, pipelining with RISC as well as RISC and Cache.	**Unit VII: RISC** 7.1 RISC and CISC systems 7.2 RISC instructions 7.3 Processor to memory movement 7.4 Pipelining with RISC 7.5 RISC and Cache	**8**
• Illustrate parallel processing and pipelining. • Explain different pipelining techniques and their hazards.	**Unit VIII: Pipelining Techniques** 8.1 Parallel processing 8.2 Introduction to pipelining 8.3 Arithmetic pipelining 8.4 Instruction pipelining 8.5 RISC pipelining 8.6 Pipelining Hazards	**12**

• Illustrate different types of network architecture and their applications.	**Unit IX: Multiprocessors** 9.1 Characteristics of multiprocessors 9.2 Flynn's classification 9.3 Enslow's classification 9.4 Interconnection structures 9.5 Cache coherence	**6**

Note: The figure in the parenthesis indicate approximate number of periods allocated for respective units.

Part II: Practical

Laboratory Work:

1. Add of two unsigned integer binary number
2. Multiplication of two unsigned integer binary numbers by Partial-Product method
3. Subtraction of two unsigned integer binary number
4. Division using restoring
5. Division using non-restoring methods
6. To simulate a direct mapping cache
7. The student should develop a project on computer Architecture. The topic could be either initiated by the student or selected from a list provided by the instructor. An oral presentation with a demonstration should be part of the laboratory project report.

4 Instructional Techniques

The instructional techniques for this course are divided into two groups. First group consists of general instructional techniques applicable to most of the units. The second group consists of specific instructional techniques applicable to specific units.

4.1 General Techniques

- Providing the reading materials to the students to familiarize the units.
- Lecture, question-answer, discussion, brainstorming, practical, and buzz session.

4.2 Specific Instructional Techniques

Unit	Activity and instructional techniques	Teaching Hours (30)
I to IX	Lecture, Discussion, Practical	

Note: ***Specific Instructional Techniques may or may not require for each of the units mentioned in course outline.***

5 Evaluation

5.1 Internal Evaluation 30%

Internal evaluation will be conducted by course teacher based on following activities:

1) Attendance	4 points
2) Participation in learning activities	6 points
3) First assignment/midterm exam	10 points
4) Second assignment/assessment (1 or two)	10 points
Total	30 points

Note: ***First assignment/assessment might be mid-term exam + assigns or book review or article review or first term paper on specific issue/topic, mid-term exam or unit test and quiz etc according to nature of course. Second assignment/assessment might be project work, case study, seminar, survey/field study and individual/group report writing, term paper based on secondary data or review of literature and documents etc.***

First and second assignment/assessment may include one or two types of assessment. For instance, one home assignment/book/article review + mid-term exam or only mid-term exam. In the second assessment may include only one project work/term paper or two type of assignment according to nature of the course.

5.2 External Evaluation (Final Examination) 70%

Examination Division, office of the Dean, Faculty of Education will conduct final examination at the end of semester (proposed).

1) Objective type question (Multiple choice 11x11)	11 points
2) Short answer questions (5 questions x 7 points)	35 points
3) Long answer questions (2 questions x 12 points)	24 points
Total	70 points

6 Recommended books and reading materials (including relevant published articles in national and international journals)

1. W. Stalling, Computer Organization and Architecture 17 edition, Prentice-Hall India Limited, New Delhi.

2. A.J Vande Goor, Computer Architecture and Design, Addison Wesley; Wokingham, UK, 1989

3.A.S Tanenbaum, Structured Computer Organization, Prentice Hall India Limited, new Delhi.
4.M.Morris Mano: Computer System Architecture, Latest Edition.
5.John P. Hayes: Computer Architecture and Organization, Latest Edition.

Author (Year of publication). Title of books. Place and publisher. (…… chapter for ….unit).
Author (Year of publication). Title of article, Name of Journal. Vol. Number, Page number (For ….. unit)

7 Reference materials

Note: *Curriculum designers are requested to provide copies of books and reading materials referred in the courses.*